GIET POLYTECHNIC JAGATPUR,CUTTACK

LESSON PLAN

Discipline : ELECTRICAL ENGG.	Semester: 5th Sem	Name of the Teaching Faculty : JYOTIRMAYA SAMAL
Subject : Digital Etc &M.P	No. of Days / per week class allotted : 05	Semester From date :01.10.2021 To Date :13.01.2022 No. of Weeks : 15
Week	**Class Day**	**Topics**
1ST	1st	1. BASICS OF DIGITAL ELECTRONIC 1.1 Binary, Octal, Hexadecimal number systems and compare with Decimal system
	2nd	1.2 Binary addition, subtraction, Multiplication and Division.
	3rd	1.3 1's complement and 2's complement numbers for a binary number
	4th	1.4 Subtraction of binary numbers in 2's complement method.
	5th	1.5 Use of weighted and Un-weighted codes & write Binary equivalent numberfor a number in 8421, Excess-3 and Gray Code and vice-versa
2ND	1st	1.6 Importance of parity Bit.
	2nd	Problems discussion
	3rd	1.7 Logic Gates: AND, OR, NOT, NAND, NOR and EX-OR gates with truth table.
	4th	1.8 Realize AND, OR, NOT operations using NAND, NOR gates.
	5TH	Revision
3RD	1st	1.9 Different postulates and De-Morgan's theorems in Boolean algebra.
	2nd	1.10 Use Of Boolean Algebra For Simplification Of Logic Expression
	3rd	1.11 Karnaugh Map For 2,3,4 Variable, Simplification Of SOP And POS Logic Expression Using K-M
	4th	1.11 Karnaugh Map For 2,3,4 Variable, Simplification Of SOP And POS Logic Expression Using K-M
	5th	1.11 Karnaugh Map For 2,3,4 Variable, Simplification Of SOP And POS Logic Expression Using K-M
4TH	1st	COMBINATIONAL LOGIC CIRCUIT 2.1 Give the concept of combinational logic circuits.
	2nd	2.2 Half adder circuit and verify its functionality using truth table.
	3rd	2.3 Realize a Half-adder using NAND gates only and NOR gates only.
	4th	2.4 Full adder circuit and explain its operation with truth table.
	5th	Problems discussion

5TH	1st	2.5 Realize full-adder using two Half-adders and an OR – gate and write truth table
	2nd	2.6 Full subtractor circuit and explain its operation with truth table.
	3rd	2.6 Full subtractor circuit and explain its operation with truth table.
	4th	2.7 Operation of 4 X 1 Multiplexers and 1 X 4 demultiplexer
	5th	2.7 Operation of 4 X 1 Multiplexers and 1 X 4 demultiplexer
6TH	1st	Problems discussion
	2nd	Revision
	3rd	2.8 Working of Binary-Decimal Encoder & 3 X 8 Decoder.
	4th	2.8 Working of Binary-Decimal Encoder & 3 X 8 Decoder.
	5th	2.9 Working of Two bit magnitude comparator.
7TH	1st	SEQUENTIAL LOGIC CIRCUITS3.1 Give the idea of Sequential logic circuits
	2nd	3.2 State the necessity of clock and give the concept of level clocking and edge triggering,
	3rd	3.3 Clocked SR flip flop with preset and clear inputs.
	4th	3.5 Construct level clocked JK flip flop using S-R flip-flop and explain with truth table
	5th	3.6 Concept of race around condition and study of master slave JK flip flop.
8TH	1st	3.7 Give the truth tables of edge triggered D and T flip flops and draw their symbols.
	2nd	3.8 Applications of flip flops. 3.9 Define modulus of a counter
	3rd	3.10 4-bit asynchronous counter and its timing diagram.3.11 Asynchronous decade counter.
	4th	3.12 4-bit synchronous counter.3.13 Distinguish between synchronous and asynchronous counte
	5th	3.14 State the need for a Register and list the four types of registers.
9TH	1st	3.15 Working of SISO, SIPO, PISO, PIPO Register with truth table using flip flop.
	2nd	Problems discussion
	3rd	Problems discussion
	4th	Revision
	5th	Revision
10TH	1st	**8085 MICROPROCESSOR:.4.1 Introduction to Microprocessors, Microcomputers**
	2nd	4.2 Architecture of Intel 8085A Microprocessor and description of each block.
	3rd	4.3 Pin diagram and description.
	4th	4.4 Stack, Stack pointer & stack top
	5th	4.5 Interrupts

11TH	1st	4.6 Opcode & Operand,
	2nd	4.7 Differentiate between one byte, two byte & three byte instruction with example.
	3rd	4.7 Differentiate between one byte, two byte & three byte instruction with example.
	4th	4.7 Differentiate between one byte, two byte & three byte instruction with example.
	5th	4.8 Instruction set of 8085 example
12TH	1st	4.8 Instruction set of 8085 example
	2nd	4.9 Addressing mode
	3rd	4 .10 Fetch Cycle, Machine Cycle, Instruction Cycle, T-State
	4th	4 .10 Fetch Cycle, Machine Cycle, Instruction Cycle, T-State
	5th	4.11 Timing Diagram for memory read, memory write, I/O read, I/O write
13TH	1st	4.11 Timing Diagram for memory read, memory write, I/O read, I/O write
	2nd	4.12 Timing Diagram for 8085 instruction
	3rd	4.13 Counter and time delay.
	4th	4. 14 Simple assembly language programming of 8085.
	5th	Revision
14TH	1st	5. INTERFACING AND SUPPORT CHIPS5.1 Basic Interfacing Concepts, Memory mapping .
	2nd	5.1 Basic Interfacing Concepts, I/O mapping
	3rd	5.2 Functional block diagram and description of each block of Programmable peripheral interface Intel 8255
	4th	5.2 Functional block diagram and description of each block of Programmable peripheral interface intel 825
	5th	5.2 Functional block diagram and description of each block of Programmable peripheral interface intel 825
15TH	1st	5.3 Application using 8255: Seven segment LED display
	2nd	5.3 Application using 8255: , Square wave generator
	3rd	5.3 Application using 8255: , Traffic light Controller
	4th	Revision
	5th	Revision